

Agenda

14th Power Analysis & Design Symposium - April 9th, 2025



	Central European Summer Time (CEST/UTC +2) (Vienna, Berlin)	Eastern Daylight Time (EST/UTC-4) (New York)	Hong Kong Time (HKT/UTC+8)
<i>Welcome and introduction</i>	09:00 / 09:00 am	03:00 am	15:00 / 03:00 pm
Simulating Power Factor Correction Stages in Single- and Three-Phase Networks by Christophe Basso - Future Electronics	09:10 / 09:10 am	03:10 am	15:10 / 03:10 pm
<i>10 min break</i>			
Inductor Resonances and Electromagnetic Interference (EMI) by Arturo Mediano - University of Zaragoza	10:20 / 10:20 am	04:20 am	16:20 / 04:20 pm
<i>10 min break</i>			
Imagine low ESL - Developing Film Capacitor with low Inductance using Bode 100 by Axel Schmidt - Yageo	11:20 / 11:20 am	05:20 am	17:20 / 05:20 pm
<i>1.5 h break</i>			
Loop Gain Measurements in Power Electronics - from POL to PFC by Florian Hämmerle - OMICRON Lab	13:40 / 01:40 pm	07:40 am	19:40 / 07:40 pm
<i>10 min break</i>			
Op-amps: Measurements and Modeling by Jan Petrik - Freelance Engineer	14:40 / 02:40 pm	08:40 am	20:40 / 08:40 pm
<i>10 min break</i>			
Calibration, Embedding & De-Embedding – Achieving Highly Accurate Impedance Results by Steve Sandler - Picotest	15:40 / 03:40 pm	09:40 am	21:40 / 09:40 pm
<i>Discussion & Closing</i>			